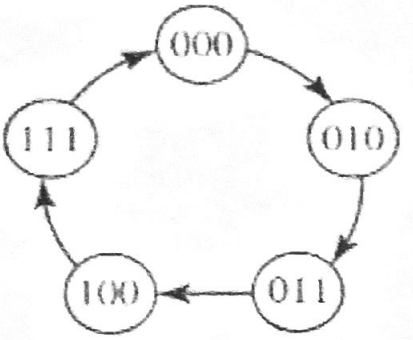
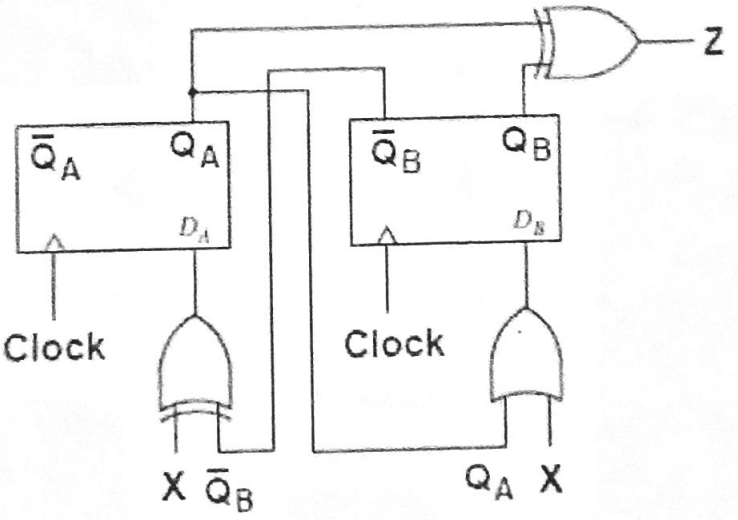
Vivekananda College of Engineering & Technology, Puttur [A Unit of Vivekananda Vidyavardhaka Sangha Puttur ®] Affiliated to VTU, Belagavi & Approved by AICTE New Delhi			
CRM08	Rev 1.10	CS/AI	10/03/22

CONTINUOUS INTERNAL EVALUATION - 3

Dept: **CS**	Sem / Div: **3 CS A/B**	Sub: **Analog and Digital Electronics**	S Code: **18CS33**
Date: 17/03/2022	Time: 9:30-11:00 am	Max Marks: 50	Elective: N

Note: Answer any 2 full questions, choosing one full question from each part.

QN		Questions	Marks	RBT	CO's
		PART A			
1	a	Derive the characteristics equations for T, SR and JK flip flops.	9	L3	CO3
	b	Explain D flip-flop with timing diagram. Give the implementation of T flip flop from D flip flop.	8	L3	CO3
	c	Explain the application of SR latch in switch debouncing technique.	8	L3	CO3
		OR			
2	a	Construct SR latch using NAND gates and derive the characteristics equation for the same.	9	L3	CO3
	b	Explain T flip flop with timing diagram. Realize T flip flop from JK flip flop.	8	L3	CO3
	c	Explain master-slave JK flip flop operation with suitable diagrams.	8	L3	CO3
		PART B			
3	a	Design Mod 5 counter using JK flip flop.	9	L3	CO4
	b	With neat diagram, Explain the working of N-bit parallel adder with accumulator.	8	L3	CO4

	c	With the help of state graph, state and transition tables and timing diagram, explain sequential parity checker.	8	L3	CO4
		OR			
4	a	Design a random counter using T flip flop, whose transition graph is shown below 	9	L3	CO4
	b	With neat diagram, explain 4 bit SISO shift register.	8	L3	CO4
	c	Differentiate between Moore and Mealy machines. Analyze the following Moore sequential circuit for an input sequence of X=01101 and draw the timing diagram. 	8	L3	CO4

11/03/22
HOD

Prepared by: Govindaraj P

10/03/22